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10/511,512	10/14/2004	Jeroen Anton Johan Leijten	NL02 0321 US	4657

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NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
GIROUX, GEORGE	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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ip.department.us@nxp.com

Continuation of 11. NOTE:

The amendments made to claim 1 overcome the rejection of claims 1-7 under 35 U.S.C. 112, second paragraph. The rest of the rejections of claims 1-7, in the action mailed 18 February 2010, remain in this case, for the reasons given below.

Applicant's arguments filed 15 April 2010 have been fully considered but they are not persuasive.

Applicant argues that the cited references do not teach the claimed invention "as a whole", and do not teach "a second set of issue slots that have holdable registers on the single data input path of an input routing network and that do not have holdable registers on the multiple data output paths of the input routing network".

However, Garde teaches that operand latch 132 holds the output of the registers 130 on the input to the routing network of op busses 110 and 112 to the computation units (column 6, lines 3-14 and figure 2), which is not on the inputs of the ALUs (i.e. the multiple data output paths) and, for the reasons given in the rejections, it would have been obvious to one of ordinary skill in the art to combine these latches on some slots with those taught by Dally, which hold data on the multiple data output paths on other slots.

/George D Giroux/
Examiner, Art Unit 2183

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183